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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,094	03/26/2004	Mark D. Matson	BP 3197	8200

34399 7590 06/06/2007

GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
WENDELL, ANDREW	
ART UNIT	**PAPER NUMBER**
2618	

MAIL DATE	DELIVERY MODE
06/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,094	MATSON ET AL.	
	Examiner	Art Unit	
	Andrew Wendell	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 11-18 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 11-18 are drawn to a "program" per se as recited in the preamble and as such is non-statutory subject matter. See MPEP 2106.IV.B.1.a. Data structures not claimed as embodied in computer readable media are descriptive material per se and are not statutory because they are not capable of causing functional change in the computer. See, e.g., Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claim aspects of the invention, which permit the data structure's functionality to be realized. In contrast, a claimed computer readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory. Similarly, computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and

other claimed elements of a computer, which permit the computer program's functionality to be realized. Note, "computer readable medium encoded with a computer program" would make the claim statutory.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-6, 10-11, and 13-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shohara et al. (US Pat# 6,473,607).

Regarding claim 1, Shohara's communication device with a self-calibrating sleep timer teaches a processing unit 42 or 50 (Fig. 1); an instruction pipeline circuit (Col. 5 lines 21-32); at least one processing module 42 or 50 (Fig. 1); a timer for generating a time-out interval 70 (Fig. 1); and power control logic 42 or 60 (Fig. 2) for detecting a sleep instruction and placing the processing unit, instruction pipeline circuit and at least one processing module in a low-power state (Col. 10 lines 39-41 and Col. 12 lines 52-64), where the power control logic is operative in response to a wake-up signal (Col. 6 line 59-Col. 7 line 32) to reactivate the instruction pipeline circuit, and consequently at least one processing module only to the extent required by the wake-up signal (Col. 12 lines 32-64, Col. 13 lines 11-13, and Col. 13 lines 61-65).

Regarding claim 2, Shohara teaches where the instruction pipeline circuit comprises a multi-stage instruction pipeline circuit (Col. 5 lines 21-32).

Regarding claim 4, Shohara teaches where the power control logic comprises instruction decode logic to detect the sleep instruction (Col. 6 line 59-Col. 7 line 32).

Regarding claim 5, Shohara teaches where the power control logic comprises branch condition logic to respond to the wake-up signal (Col. 6 line 59-Col. 7 line 32).

Regarding claim 6, Shohara teaches where the power control logic, having specified one or more wake-up conditions that the processing unit will respond to when in a low-power state, generates the wake-up signal upon detecting the one or more wake-up conditions or the time-out interval (Col. 6 line 59-Col. 7 line 32 and Col. 12 lines 32-64).

Regarding claim 8, Shohara teaches where the power control logic instructs the instruction pipeline circuit to cease fetching new instructions after encountering a sleep instruction whose wake-up conditions are currently deasserted (Col. 5 lines 21-64,Col. 10 lines 39-41, Col. 12 lines 52-64, and Col. 14 line 65-Col. 15 line 7).

Regarding claim 10, Shohara teaches wherein the wake-up conditions and time-out interval are stored in a register by the power control logic (Col. 6 line 59-60 and Col. 5 lines 21-26).

Regarding claim 11, recordable medium claim is rejected for the same reason as apparatus claim 1 since the recited elements would perform the claimed steps.

Regarding claim 13, Shohara teaches wherein the instruction pipeline comprises a multistage instruction pipeline, and the processing device reactivates only stages in the multistage instruction pipeline and/or the function units needed to process one or

more instructions necessary to analyze and respond to the wake-up signal (Col. 5 lines 21-32).

Regarding claim 14, Shohara teaches a register for holding the specified wake-up conditions and time out signal.

Regarding claim 16, Shohara teaches where the executable instructions and data comprise control logic 60 (Fig. 2) for controlling the operation of the processing device (Col. 15 lines 37-39).

Regarding claim 17, Shohara teaches where the processing device powers down the one or more processor modules by freezing a clock signal for said one or more modules (Col. 12 lines 52-56).

Regarding claim 18, Shohara teaches where the processing device powers down the one or more processor modules by placing said one or more modules in an idle mode (Col. 12 lines 52-56).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shohara et al. (US Pat# 6,473,607) in view of Fukuhara (US Pat Pub# 2003/0028677).

Regarding claim 3, Shohara's communication device with a self-calibrating sleep timer teaches the limitations in claim 1. Shohara fails to teach a logical OR.

Fukuhara's network device teaches where the wake-up signal comprises a logical OR combination (Section 0016).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a logical OR as taught by Fukuhara into Shohara's communication device with a self-calibrating sleep timer in order to reduce the consumption of unnecessary electric power (Section 0027).

6. Claims 7, 12, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shohara et al. (US Pat# 6,473,607) in view of Lindskog et al. (US Pat# 6,622,251).

Regarding claim 7, Shohara's communication device with a self-calibrating sleep timer teaches the limitations in claim 1. Shohara fails to teach completing any instructions before sleep mode.

Lindskog's mobile terminal teaches where the power control logic instructs the instruction pipeline circuit to complete any instructions preceding the sleep instruction (Col. 2 lines 48-65 and Col. 4 lines 44-55).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate completing any instructions before sleep mode as taught by Lindskog into Shohara's communication device with a self-calibrating sleep timer in order to improve on power saving techniques (Col. 5 lines 4-17).

Regarding claim 12, the combination including Lindskog teaches wherein the processing device executes any instructions received by the instruction pipeline before the sleep instruction is received (Col. 2 lines 48-65 and Col. 4 lines 44-55).

Regarding claim 19, Shohara teaches storing one or more wake-up conditions and a time-out interval in a register 24 (Fig. 1, Col. 6 line 59-60, and Col. 5 lines 21-26); receiving a processor sleep instruction (Col. 5 lines 21-33, Col. 6 line 59- Col. 7 line 32, Col. 10 lines 39-41, and Col. 12 lines 52-64); executing any pending instructions received by the processor before the sleep instruction (Col. 5 lines 21-64); powering down the one or more processor modules (Col. 5 lines 21-33, Col. 6 line 59-Col. 7 line 32, Col. 10 lines 39-41, and Col. 12 lines 52-64); receiving a processor wake-up signal corresponding to one of said wake-up conditions or said time-out interval (Col. 6 line 59-Col. 7 line 32); powering up only the processor modules required to respond to the detected processor wake-up signal (Col. 6 line 59-Col. 7 line 32, Col. 12 lines 32-64, Col. 13 lines 11-13, and Col. 13 lines 61-65). Shohara fails to teach executing any pending instructions received by the processor before the sleep instruction.

Lindskog teaches executing any pending instructions received by the processor before the sleep instruction (Col. 2 lines 48-65 and Col. 4 lines 44-55).

Regarding claim 20, the combination including Shohara teaches wherein one of the processor modules comprises an instruction pipeline circuit (Col. 5 lines 21-32).

7. Claims 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shohara et al. (US Pat# 6,473,607) in view of Karaoguz et al. (US Pat Pub# 2002/0059434).

Regarding claim 9, Shohara's communication device with a self-calibrating sleep timer teaches the limitations in claim 1. Shohara fails to teach using CMOS processing.

Karaoguz's communication device teaches a circuit and at least one processing module are formed together on a common silicon substrate using CMOS processing (Section 0071).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate using CMOS processing as taught by Karaoguz into Shohara's communication device with a self-calibrating sleep timer in order to communicate with a variety of networks (Section 0008).

Regarding claim 15, the combination including Karaoguz teaches where the processing device is implemented as part of a single-chip wireless communication device (Section 0071).

Response to Arguments

Applicant's Remarks	Examiner's Response
"Applicants respectfully submit that the claim rejections completely ignore the specific language of the claims that recite selective reactivation of the instruction	In Col. 6 line 59-Col. 7 line 32 of Shohara it clearly states that based on a wake up signal it powers up control logic circuit (instruction pipeline) and selectively power

pipeline and one or more of the processing modules to the extent required by the received wake-up signal."	up or power down components (i.e. receiver, control circuits, storage mediums) of the device.
"However, a careful reading of the cited passage confirms that Shohara nowhere discloses an "instruction pipeline circuit," much less an instruction pipeline circuit which is selectively powered down and up in response to sleep instructions and wake-up signals."	Shohara discloses an instruction pipeline in Col. 5 lines 21-32 or Col. 6 line 59-Col. 7 line 32. Any circuit that carries out instructions (i.e. control information) to other components through channels (i.e. connections) can be considered an instruction pipeline given the broadest responsible interpretation.
"Nor will Applicants elaborate upon the erroneous rejections of claims 9 and 15, other than to note that both of the Shohara and Karaoguz references used to reject these claims were commonly owned by the assignee of the present invention, namely Broadcom Corporation."	Both Shohara and Karaoguz were published a year before the filling date of the application.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Wendell whose telephone number is 571-272-0557. The examiner can normally be reached on 7:30-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 571-272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew Wendell
Examiner
Art Unit 2618

5/14/2007

NAY MAUNG
SUPERVISORY PATENT EXAMINER